Riviera-PRO™ | Advanced Verification

Verification Platform

Riviera-PRO™ addresses verification needs of engineers crafting tomorrow's cutting-edge FPGA and SoC devices. Riviera-PRO enables the ultimate testbench productivity, reusability, and automation by combining the high-performance simulation engine, advanced debugging capabilities at different levels of abstraction, and support for the latest Language and Verification Library Standards.

Verification Platform that grows with your requirements.

System Interfaces
MATLAB®, SystemVue®

Debugging Mixed-Language
IDE, Code tracing, Waveform, Dataflow

Metrics Coverage, Assertions
Code & Functional Coverage, SVA/PSL/OVA

Test Automation TLM, RTL, Gate-Level
SystemVerilog, SystemC, UVM, C/C++

Simulation Mixed-Language, Mixed-Signal, HW/SW
Verilog, Verilog-AMS, VHDL

Top Benefits

Standards-based support for VHDL, SystemVerilog, and SystemC to enable design and verification of the most sophisticated digital designs

High-performance simulator with industry-leading capacity and high regression throughput for developing complex systems

Integrated multi-language debug environment to automate time-consuming design analysis tasks and fix bugs quickly

Comprehensive assertion-based verification (SVA, PSL, and OVA) for increased design observability and decreased debug time

Advanced code coverage capabilities and coverage analysis tools for fast metric-based verification closure
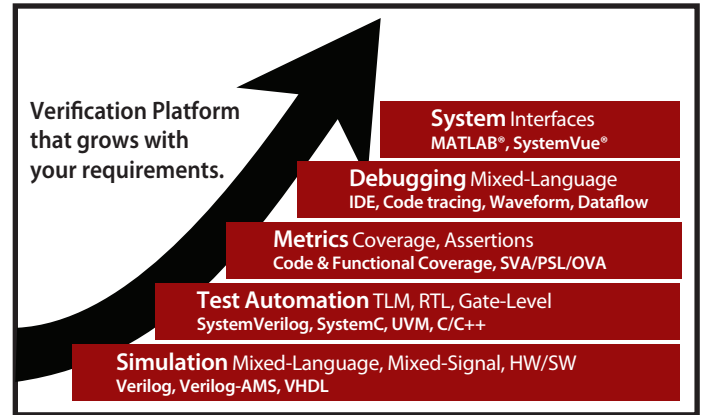
High Performance Simulation

Riviera-PRO incorporates industry-leading simulation optimization algorithms to achieve the highest performance in mixed-language simulations. Combined with the industry-leading capacity, Riviera-PRO enables high regression throughput for developing the most complex systems.

Advanced Debugging

Integrated multi-language debug environment enables automating time-consuming design analysis tasks and fixing bugs quickly. It supports all standard languages and provides intuitive ways to visualize and analyze key objects in your design. Built-in debugging tools provide code tracing, waveform, dataflow, coverage, assertion, and memory visualization capabilities.

Industry's Best ROI

Riviera-PRO enables Aldec customers to deliver innovative products at a lower cost in shorter time. Aldec's proven design automation methods help customers to speed up the design and implementation of products for automotive, medical, aerospace, and military applications. In addition to EDA tool packages accompanied by the comprehensive trainings and support, Aldec invests in the partnerships and integrations necessary to build complete design and verification flows.

ALDEC
THE DESIGN VERIFICATION COMPANY

FEATURES

PRODUCT CONFIGURATIONS

Supported Standards	LV	LVT	LVT-SV
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	•	•	•
Verilog® HDL IEEE 1364 (1995, 2001 and 2005)	•	•	•
SystemVerilog IEEE 1800™-2009 (Design)	•	•	•
SystemC™ 2.2 IEEE 1666™/OSCI 2.2/TLM 2.0	Option	•	•
Analog/Mixed Signal (SPICE, Verilog-AMS 2.3.1)		Option	Option
SystemVerilog IEEE 1800™-2009 (Verification)			•
Verification Libraries (UVM/OVM and VMM)			•
Design Entry and Design Management			
HDL Editor with Auto-Complete and Code Templates	•	•	•
File Browser, Design and Library Managers	•	•	•
Customizable GUI Perspectives	•	•	•
Project Tasks Management	•	•	•
Macro, Tcl/Tk, Perl script support	•	•	•
HDL Debug and Analysis			
Interactive Code Execution Tracing	•	•	•
Advanced Breakpoint Management	•	•	•
Accelerated Waveform Viewer (ASDB)	•	•	•
Hierarchical References to/from VHDL (Signal Agent)	•	•	•
Post-Simulation Debug	•	•	•
Waveform Compare	•	•	•
Assertions in Waveform and Debugging	Option	•	•
Memory Viewer	•	•	•
Integrated C/SystemC Debugger		•	•
X-Trace	Option	•	•
Advanced Dataflow	Option	•	•
Simulation/Verification			
Single or Mixed Language	•	•	•
Verilog Programming Language Interfaces (PLI/VPI)	•	•	•
VHDL Programming Language Interface (VHPI)	•	•	•
SystemVerilog IEEE 1800™-2005 DPI 2.0	•	•	•
Value Change Dump (VCD and Extended VCD) Support	•	•	•
Incremental Compilation	•	•	•
Multi-Threaded Compilation	•	•	•
32/64-Bit Cross-Compatible Libraries	•	•	•
Simulation Model Protection/Library Encryption	•	•	•
VHDL 2008 and Verilog 2005 IEEE Encryption	•	•	•
Xilinx® SecureIP Support	Option	•	•
Altera® Language-Neutral Libraries	Option	•	•
Simulation Performance Optimization (Verilog/SystemVerilog, VHDL)		•	•
64-bit Simulation		•	•
Transaction-Level Visual Debugging		Option	•
Profiler (Performance Metrics)	Option	•	•
SFM (Server Farm Manager)	Option	Option	•
HES™ Hardware Assisted Verification (Acceleration and Emulation)	Option	Option	Option
Assertions and Coverage Tools			
PSL, SystemVerilog, OpenVera Assertions and Functional Coverage (Assertion)	Option	•	•
Code and Toggle Coverage and UCIS-compatible Aldec Coverage Database	Option	•	•
Functional Coverage (Covergroup)			•
External Simulation Interfaces			
Synopsys® SmartModels, SWIFT Interface and LMTV	Option	•	•
SpringSoft® Verdi™ FSDB Recording	Option	•	•
Co-Simulation Interfaces			
Agilent SystemVue®	•	•	•
MathWorks Simulink®"	•	•	•
MathWorks MATLAB®"	Option	•	•
Design Rule Checking			
ALINT™ with Aldec Basic Rule Library	Option	•	•
DO-254 VHDL or Verilog Rule Library	Option	Option	Option
STARC® VHDL or Verilog Rule Library	Option	Option	Option
Reuse Methodology Manual (RMM) Rule Library	Option	Option	Option
Supported Platforms			
Windows® 7/Vista/XP/2003 32/64 bit	32-Bit Only	•	•
Linux 32/64 bit	32-Bit Only	•	•