Active-HDL™ | FPGA Design and Simulation

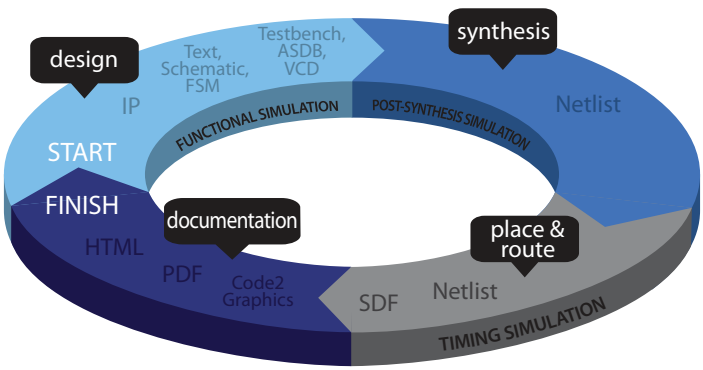
Design Creation and Simulation

Active-HDL™ is a Windows® based, integrated FPGA Design Creation and Simulation solution for team-based environments. The Integrated Design Environment (IDE) within Active-HDL includes a full HDL and graphical design tool suite and RTL/gate-level mixed language simulator for rapid deployment and verification of FPGA designs. The design flow manager evokes over 120 EDA and FPGA tools, during design entry, simulation, synthesis and implementation flows and allows teams to remain within one common platform during the entire FPGA development process. Active-HDL supports industry leading FPGA devices from Altera®, Atmel®, Lattice®, Microsemi™ (Actel), Quicklogic®, Xilinx® and more.

Top Benefits

- **Unified Team-based Design Management**
- **Deploy designs quickly with Text, Schematic and State Machine**
- **Powerful common kernel mixed-language simulator (VHDL, Verilog, SystemVerilog (Design), SystemC)**
- **Advanced Debugging and Code Coverage**
- **Assertion-Based Verification (SVA, PSL, OVA)**
- **DSP Co-simulation with MATLAB®/Simulink® interface**
- **Share designs quickly with auto-generate Design Documentation in HTML and PDF**

FPGA Design Flow



Design

The Design Suite within Active-HDL utilizes graphical and textual design entry methods, and integrates over 120 EDA tools into a single platform. Design management tools help eliminate issues faced by team-based designs during the FPGA developement process.

Debug

Active-HDL incorporates a common kernel mixed-language simulator with interactive tools that enables designers to debug quickly. Debugging tools such as Advanced Data Flow and Xtrace provide users a graphical representation of the system's internal signals increasing observability and aiding in the debug of large designs. Active-HDL also includes Code Coverage and Analysis tools, allowing designers to incorporate metric-driven verification into the design process.

Document

Active-HDL allows designers to quickly document all aspects of their design workspace for later review, reuse, and archiving. This enables the ability to maintain proper documentation at all stages of the development process, eliminating many issues faced by multi-team design environments.

ALDEC®
THE DESIGN VERIFICATION COMPANY

STANDARDS

accellera
EDA CONSORTIUM
IEEE
SYSTEMC™
SystemVerilog

SILICON

achronix SEMICONDUCTOR CORPORATION
ALTERA
LATTICE SEMICONDUCTOR
Microsemi
tabula
QuickLogic
XILINX

INTERFACES

ARM
Altium
cadence
The MathWorks
Mentor Graphics
SYNOPSYS
ZUKEN

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FEATURES

PRODUCT CONFIGURATIONS

Design Entry and Documentation	DM	Designer Edition	PE	EE
HDL, Text, Block Diagram and State Machine Editor	•	•	•	•
Language Assistant with Templates and Auto-Complete	•	•	•	•
Macro, Tcl/Tk, Perl script Support	•	•	•	•
Mouse Strokes	•	•	•	•
Code2Graphics™ Converter	•		•	•
Legacy Schematic Design Import and Symbol Import/Export	•		•	•
Export to PDF/HTML/Bitmap Graphics	•		•	•
Advanced Export to PDF (Vector Graphics)	Option		•	•
Project Management				
Design Flow Manager for All FPGA Vendors	•	•	•	•
Revision Control Interface	•	•	•	•
Team-based Design Management	•	•	•	•
PCB Interface			•	•
Code Generation Tools				
IP Core Component Generator	•		•	•
Testbench Generation from Waveforms			•	•
Testbench Generation from State Diagram			•	•
Supported Standards				
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	•	•	•	•
Verilog® HDL IEEE 1364 (1995, 2001 and 2005)	•	•	•	•
SystemVerilog IEEE 1800™-2005 (Design)	•	•	•	•
EDIF 2 0 0			•	•
SystemC™ 2.2 IEEE 1666™/OSCI 2.2/TLM 2.0			Option	•
Simulation/Verification				
Simulation Performance (Baseline 2X Faster than FPGA Vendor Supplied Simulator)		Baseline	3X Baseline	Up To 6X Baseline
Single or Mixed Language Design Support	Mixed Only	Mixed Only	•	•
Simulation Model Protection/Library Encryption		•	•	•
VHDL/Verilog IEEE Compatible Encryption		•	•	•
Value Change Dump (VCD and Extended VCD) Support		•	•	•
Verilog Programming Language Interface(PLI/VPI)		•	•	•
VHDL Programming Language Interface (VHPI)			•	•
Batch Mode Simulation/Regression (VSimSA)			•	•
Pre-compiled FPGA Vendor Libraries	•	•	•	•
Xilinx SecureIP Support		•	Option	•
Altera® Language-Neutral Libraries		•	Option	•
Profiler (Performance Metrics)			Option	•
Verilog HDL Simulation Optimization				•
VHDL Simulation Optimization				•
SFM (Server Farm Manager)			Option	Option
HDL Debug and Analysis				
Interactive Code Execution Tracing		•	•	•
Advanced Breakpoint Management		•	•	•
Memory Viewer		•	•	•
Waveform Viewer		Viewer Only	•	•
Waveform Stimulator		•	•	•
Waveform Comparison and Editing			•	•
Post-Simulation Debug			•	•
C++ Debugger			•	•
Signal Agent (VHDL and Mixed Only)			•	•
X-Trace			Option	•
Advanced Dataflow			Option	•
Integration with Riviera-PRO and ALINT	Option		Option	•
Assertions Debugging			Option	Option
Synopsys® SmartModels, SWIFT interface and LMTV			Option	•
Assertions and Coverage Tools				
UCIS-compatible Aldec Coverage Database			Option	•
Code, Statement, Branch, Expression, Condition, Path and Toggle Coverage			Option	•
PSL IEEE 1850, SystemVerilog IEEE 1800™, OpenVera Assertions			Option	Option
Design Rule Checking				
ALINT™ with Aldec Basic Rule Library			Option	•
DO-254 VHDL or Verilog Rule Library			Option	Option
STARC® VHDL or Verilog Rule Library			Option	Option
RMM Verilog and VHDL Rule Library			Option	Option
Co-Simulation				
Simulink® Co-Simulation			•	•
MATLAB® Co-Simulation			Option	•
Supported Platforms				
Windows® 7/Vista/XP/2003 32/64 bit	•	•	•	•

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