

Design Rule Checking



ALINT™

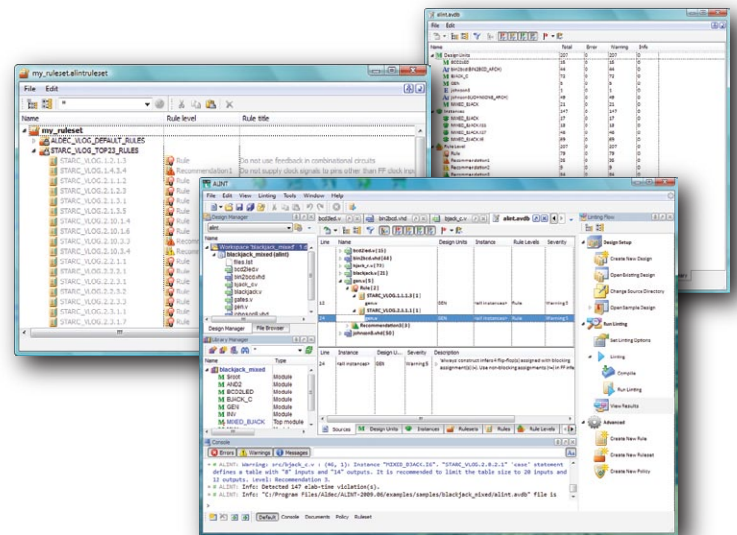
ALINT is an RTL design analysis tool, which identifies potential design issues early in the development cycle. The tool checks VHDL, Verilog® mixed-language designs for structural, coding and consistency issues prior to Simulation and Synthesis. ALINT significantly reduces verification time of complex FPGA and ASIC designs, resulting in uniform, re-usable and reliable code which reduces the risk of costly ASIC re-spins.

Top Features

- Fast Design Analysis of complex ASIC/FPGA/SOC designs
- Comprehensive Set of Design Rules
- Integrated Results Analysis and Debugging Environment
- IEEE VHDL, Verilog and Mixed-Language support
- User-defined Design Rules
- DO-254 Rule Set
- Linux and Windows® Vista/XP/2003/2000 32/64 bit support

Benefits of Design Rule Checking

Design Rule Checking provides designers with the opportunity to discover complex design issues early in the design flow before Simulation and Synthesis are performed. Design Rule Checking ensures that coding and source code management conventions are followed. It also checks code for synthesizability, to prevent potential simulation problems and eliminate differences between the results of RTL and post-synthesis simulation.



Prepackaged Design Rules

ALINT offers a set of prepackaged rules that help designers maximize performance of tools for Simulation and Synthesis. The current set of design rules consists of STARC® VHDL, STARC Verilog, Aldec DO-254 and Aldec VHDL/Verilog design rules. The areas covered by the rules include: basic design constraints, synthesizable description, reusability, synchronous design, clocks and resets, combinational logic, CDC and DFT.

Debugging and Results Analysis

ALINT features an Integrated Debugging Environment that includes an HDL Editor and Violation Viewer, which facilitates extensive results analysis and debugging. The Violation Viewer includes an advanced violations summary, cross-probing between violations reports and HDL code, filtering of violations, search, export of linting results and comparison of violation reports from two subsequent linting sessions.

STANDARDS



PARTNERS



FEATURES

PRODUCT CONFIGURATIONS

General	ALINT
Design Setup/Management	•
Integrated Debugging Environment	•
GUI Mode Execution	•
Batch Mode Execution	•
Supported Languages	
Verilog® IEEE 1364 (1995, 2001 and 2005)	•
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	•
Configuration and Setup	
Linting Flow	•
User-Defined Rules	•
Configuration Viewer	•
Rule Description Viewer	•
Rule Plug-in Viewer	•
Ruleset Editor	•
Rule Parameters Editor	•
Policy Editor	•
Results Analysis	
Violation Viewer	•
Cross-Probing to Source Code	•
Violation Reports Comparison	•
Design Rule Libraries	
Aldec Basic Rule Library	•
STARC® VHDL Rule Library	Option
STARC® Verilog Rule Library	Option
DO-254 VHDL Rule Library	Option
DO-254 Verilog Rule Library	Option
Supported Platforms	
Windows® Vista/XP/2003/2000 32/64 bit	•
Linux 32/64 bit	•

Prepackaged Design Rules

STARC® Design Rules

STARC is a consortium of 11 Japanese ASIC foundries that has established a set of design guidelines based on proven, best-design practices. The STARC RTL Design Style Guide for VHDL and Verilog, Second Edition, is used as ALINT's foundation.

Aldec Design Rules

Aldec offers a mixture of VHDL and Verilog rules which have been most commonly used by FPGA designers. This basic rule set is a starting point for any organization to run basic design checks and then customize them to organizational requirements.

DO-254 Design Rules

Available in either VHDL or Verilog, this set of rules provides a guideline for what is required as part of DO-254 compliance requirements. It is highly recommended that each organization reviews its own internal requirements with the DER to ensure achievement of compliance requirements for the specific project.

Create Custom Rules

ALINT's programming interface can be used by designers to implement their own rules as well as company-specific guidelines. An embedded C/C++ API wizard simplifies the process of creating new rules. All necessary templates are created automatically and should be completed by designers for the desired functionality. Once created, the user-defined rules are managed by the tool in the same way as prepackaged rules.

Design Management

ALINT provides a customizable framework that includes a set of powerful utilities for design management, result analysis and debugging. A Design Manager allows viewing and management of designs and their resources. The Rule Plug-in Viewer provides fast access to prepackaged rules. A Violation Viewer allows detailed and efficient analysis of results.



World Wide Web

www.aldec.com
sales@aldec.com
info@aldec.com
support@aldec.com
www.aldec.com/Downloads
www.aldec.com/Contact
www.aldec.com/Distributors

North America

2260 Corporate Circle
Henderson, NV 89074
Phone: 702.990.4400
Fax: 702.990.4414
E-mail: sales@aldec.com

Europe

70 rue Cortambert
75116 Paris, France
Phone: 33.6.80.32.60.56
Fax: 33.1.46.34.85.91
Email: sales-eu@aldec.com

Japan

JESCO Shinjyukugyoen Bldg 7F
1-8-4, Shinjyuku, Shinjyuku-ku
Tokyo 160-0022, Japan
Phone: 81.3.5312.1791
Fax: 81.3.5312.1795
Email: info@aldec.co.jp
Website: www.aldec.co.jp

China

Suite 2004, BaoAn Building
#800 DongFang Road
PuDong District
Shanghai City 200122, P.R. China
Phone: 86.21.6875.20.30
Fax: 86.21.6875.0083
Email: info@aldec.com.cn

